# Low-Dropout Voltage-Tracking LDO

**Check for Samples: TPS7B4250-Q1**

## FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C4**
- **–20-V to 45-V Wide, Maximum Input Voltage Range**
- **Output Current, 50 mA**
- **Very-Low Output-Tracking Tolerance, 5 mV (max)**
- **150-mV Low Dropout Voltage When $I_{OUT}$ = 10 mA**
- **Combined Reference and Enable Input**
- **40-µA Low Quiescent Current at Light Load**
- **Extreme, Wide ESR Range.**
  - **Stable with 1-µF to 50-µF Ceramic Output Capacitor, ESR 1 mΩ to 20 Ω**
- **Reverse Polarity Protection**
- **Overtemperature Protection**
- **Output Short-Circuit Proof to Ground and Supply**
- **SOT23 Package**

## APPLICATIONS

- **Automotive**
- **Off-board Sensor Supply**
- **High-Precision Voltage Tracking**

## DESCRIPTION

The TPS7B4250-Q1 device is a monolithic, integrated low-dropout voltage tracker. The device is available in a SOT-23 package. The TPS7B4250-Q1 device is designed to supply off-board sensors in an automotive environment. The IC has integrated protection for overload, over temperature, reverse polarity, and output short-circuit to the battery and ground.

A reference voltage applied at the adjust-input pin, ADJ, regulates supply voltages up to VIN = 45 V with high accuracy and loads up to 50 mA.

By setting the adjust/enable input pin, ADJ/EN, to low, the TPS7B4250-Q1 device switches to standby mode which reduces the quiescent current to the minimum value.

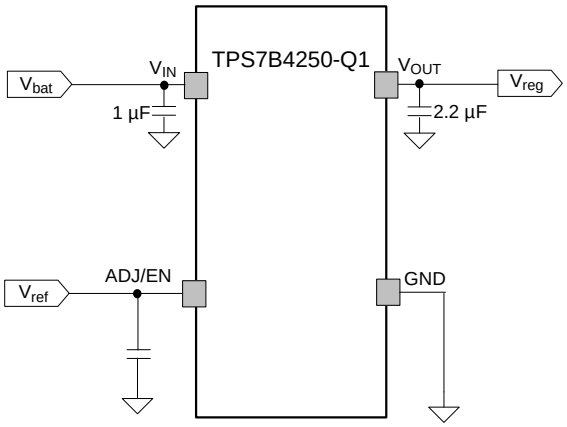



**Figure 1. Typical Application Schematic of TPS7B4250**

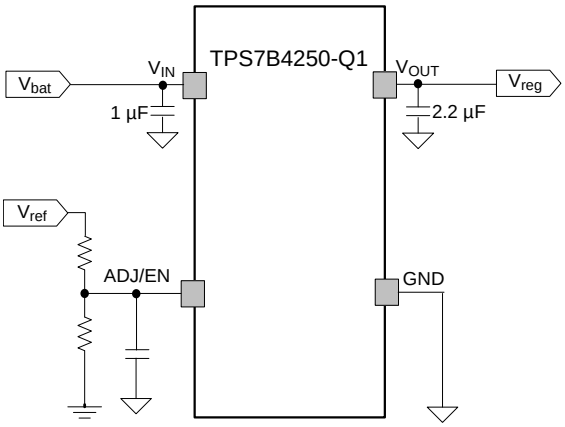



**Figure 2. Output Lower than Reference Voltage**

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage, unregulated input(2)(3) | | –20 | 45 | V |
| $V_{OUT}$ | Output voltage, regulated output | | –1 | 22 | |
| ADJ/EN | Adjust input and enable input voltage(2)(3) | | –0.3 | 22 | |
| ADJ–$V_{IN}$ | ADJ Voltage minus input voltage, $V_{IN}$ > 0 V | | | 7 | |
| ESD(4) | Electrostatic discharge | Human body model (HBM) H2(5) | | 4 | kV |
| | | Charged device model (CDM) C4 | | 1 | |
| $T_J$ | Operating junction temperature range | | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground, GND.
(3) Absolute maximum voltage.
(4) The maximum transient current flow through the internal ESD diode between GND and $V_{OUT}$ can go up to 500 mA, less than 500 µs.
(5) The human body model is a 107-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

## THERMAL INFORMATION

| THERMAL METRIC(1)(2) | | TPS7B4250-Q1 | UNIT |
|---|---|---|---|
| | | DBV 5-PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 171.7 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 81.1 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 31.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 4.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 31.2 | °C/W |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | Not Applicable | °C/W |

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) The thermal data is based on the JEDEC standard high K profile, JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.

## RECOMMENDED OPERATING CONDITIONS(1)

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Unregulated input | 4 | 40 | V |
| $V_{OUT}$ | regulated output | 1.5 | 18 | |
| ADJ/EN | Adjust input and enable input voltage | 1.5 | 18 | |
| ADJ–$V_{IN}$ | ADJ voltage minus input voltage | | 5 | |
| $C_{OUT}$ | Output capacitor requirements(2) | 1 | 50 | µF |
| $ESR_{COUT}$ | Output ESR requirements | 0.001 | 20 | Ω |
| $T_J$ | Operating junction temperature range | –40 | 150 | °C |

(1) Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.
(2) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.

## ELECTRICAL CHARACTERISTICS

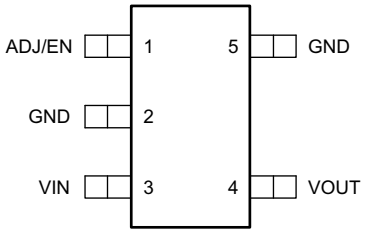
$V_I$ = 13.5 V, 18 V ≥ $V_{ADJ/EN}$ ≥ 1.5 V, $T_J$ = –40ºC to 150ºC unless otherwise stated

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{UVLO}$ | $V_{IN}$ undervoltage detection | Ramp up $V_I$ until the output turns on, $V_{ADJ}$ = 1.5 V | 3.65 | | | V |
| | | Ramp down $V_I$ until the output turns off, $V_{ADJ}$ = 1.5 V | | | 3 | |
| $\Delta V_O$ | Output-voltage tracking accuracy | $I_O$ = 100 µA to 1 mA, $V_I$ = 4 V to 40 V, 1.5 V < $V_{ADJ}$ < $V_I$ – 0.3 V | –4 | | 4 | mV |
| | | $I_O$ = 1 mA to 50 mA, $V_I$ = 4 V to 40 V, 1.5 V < $V_{ADJ}$ < $V_I$ – 1.5 V | –5 | | 5 | |
| $\Delta V_{O(\Delta IL)}$ | Load regulation steady-state | $I_O$ = 1 mA to 30 mA | | | 4 | mV |
| $\Delta V_{O(\Delta VI)}$ | Line regulation steady-state | $I_O$ = 10 mA, $V_{IN}$ = 6 V to 40 V | | | 3 | mV |
| PSRR | Power-supply ripple rejection | Frequency = 100 Hz, $V_{rip}$ = 0.5 $V_{PP}$ | | 60 | | dB |
| $V_{dropout}$ | Dropout voltage, $V_{dropout} = V_I - V_Q$ | $I_O$ = 10 mA, $V_{IN}$ ≥ 4 V (1) | | 150 | 250 | mV |
| | | $I_O$ = 50 mA, $V_{IN}$ ≥ 4 V (1) | | 550 | 1000 | |
| $I_L$ | Output-current limitation | $V_{OUT}$ short to GND | 100 | | 500 | mA |
| $I_R$ | Reverse current at $V_{IN}$ | $V_I$ = 0 V, $V_O$ = 20 V, $V_{ADJ}$ = 5 V | –5 | | 0 | µA |
| $I_{RN1}$ | Reverse current at negative input voltage | $V_I$ = –20 V, $V_O$ = 0 V, $V_{ADJ}$ = 5 V | –5 | | 0 | µA |
| $I_{RN2}$ | | $V_I$ = –20 V, $V_O$ = 20 V, $V_{ADJ}$ = 5 V | –5 | | 0 | |
| $T_{SD}$ | Thermal shutdown temperature | $T_J$ increasing because of power dissipation generated by the IC | | 175 | | °C |
| $I_Q$ | Current consumption | $V_{ADJ}$ < 0.8 V, $T_A$ ≤ 85°C (2) | | 7.5 | 15 | µA |
| | | $V_{ADJ}$ < 0.8 V, $T_A$ ≤ 125°C | | | 20 | |
| | | $I_O$ = 0.5 mA, $V_{ADJ}$ = 5 V | | 40 | 90 | |
| | | $I_O$ = 30 mA, $V_{ADJ}$ = 5 V | | 150 | 350 | |
| $I_{ADJ}$ | Adjust-input and enable-input current | $V_{ADJ}$ = 5 V | | | 1 | µA |
| $V_{ADJ,low}$ | Adjust and enable low signal valid | $V_O$ = 0 V | | | 0.8 | V |
| $V_{ADJ,high}$ | Adjust and enable high signal valid | $\lvert V_O - V_{ADJ} \rvert$ < 5 mV | 1.5 | | 18 | V |

(1) Measured when the output voltage $V_Q$ has dropped 10 mV from the typical value.
(2) Ensured by design.

## DEVICE INFORMATION

**SOT-23 (DBV) PACKAGE**
**5-PIN**
**(TOP VIEW)**




## TERMINAL FUNCTIONS

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ADJ/EN | 1 | I | This pin connects to the reference voltage. A low signal disables the IC and a high signal enables the IC. Connected the voltage reference directly or with a voltage divider for lower output voltages. To compensate for line influences, TI recommends to place a capacitor close to the IC pins. |
| GND | 2 | G | Internally connected to pin 5 |
| | 5 | | Internally connected to pin 2 |
| $V_{IN}$ | 3 | I | This pin is the IC supply. To compensate for line influences, TI recommends to place a capacitor close to the IC pins. |
| $V_{OUT}$ | 4 | O | $V_{OUT}$ is an external capacitor that is required between $V_{OUT}$ and GND with respect to the capacitance and ESR requirements given in the RECOMMENDED OPERATING CONDITIONS. |

## FUNCTIONAL BLOCK DIAGRAM

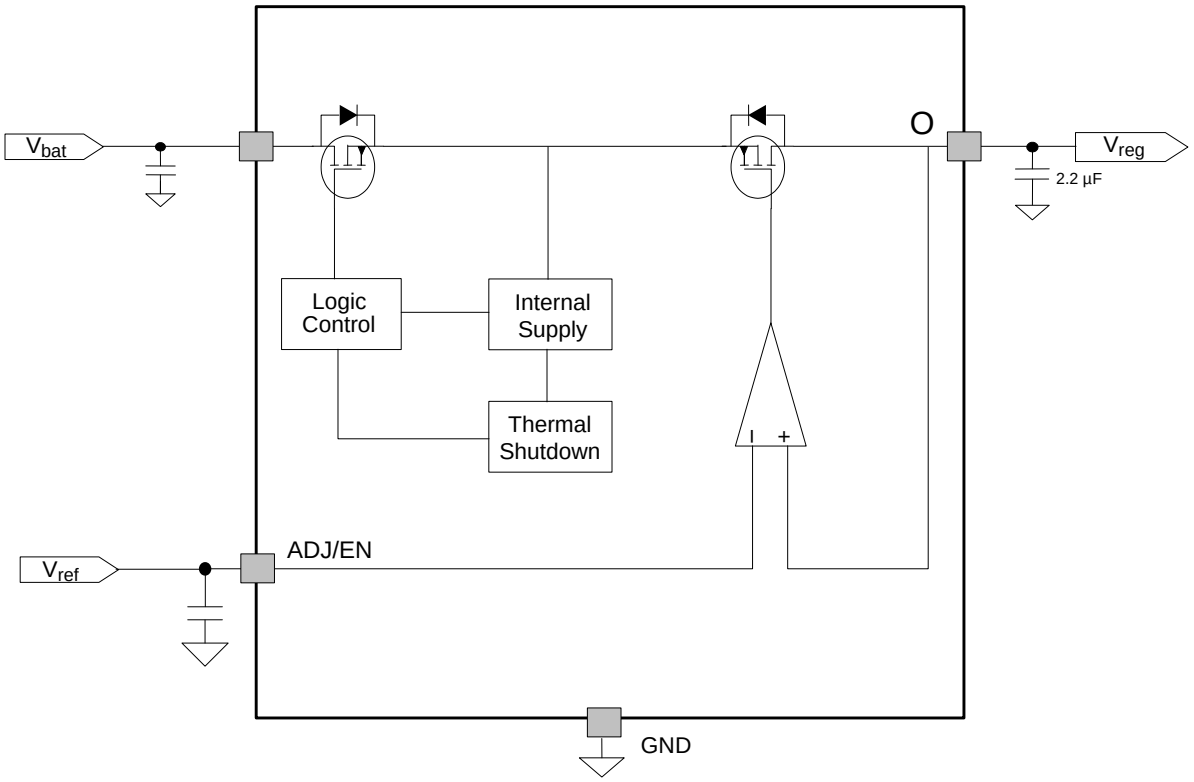



**Figure 3. TPS7B4250 Functional Block Diagram**

## TYPICAL CHARACTERISTICS

**DROPOUT VOLTAGE vs TEMPERATURE ($V_I$ = $V_{ADJ}$ = 4 V, $I_O$ = 10 mA)**

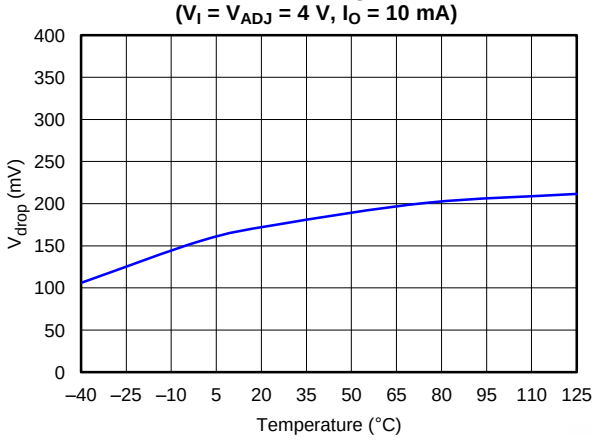



**Figure 4.**

**DROPOUT VOLTAGE vs OUTPUT CURRENT ($V_I$ = $V_{ADJ}$ = 4 V)**

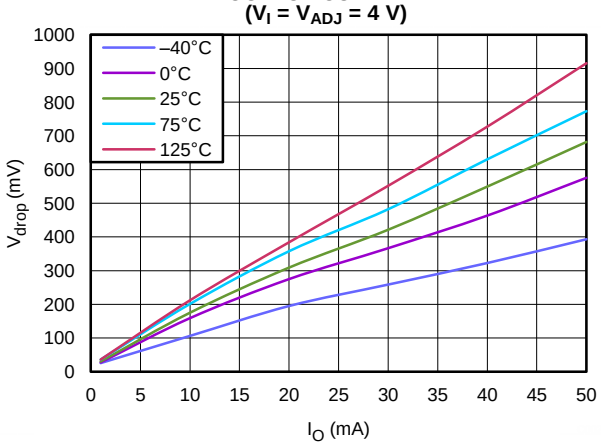



**Figure 5.**

**GROUND CURRENT vs OUTPUT CURRENT ($V_I$ = 13.5 V, $V_{ADJ}$ = 5 V)**

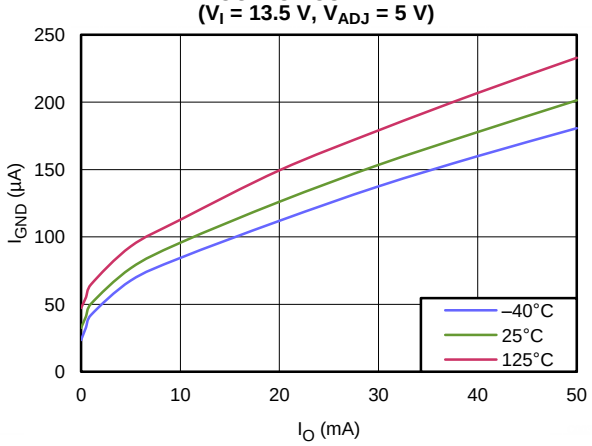



**Figure 6.**

**GROUND CURRENT vs TEMPERATURE ($V_I$ = 13.5 V)**

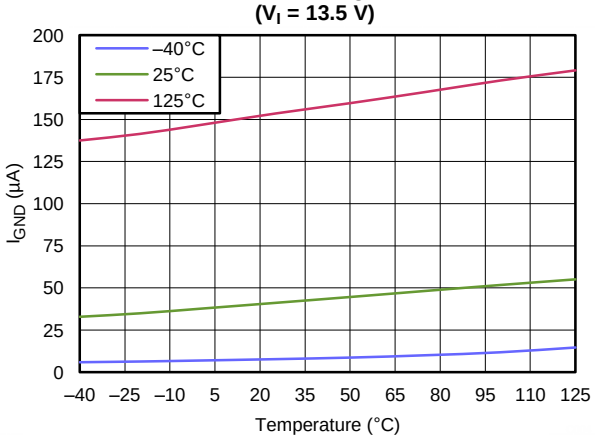



**Figure 7.**

**CURRENT-LIMIT vs TEMPERATURE ($V_I$ = 13.5 V, $V_{ADJ}$ = 5 V)**

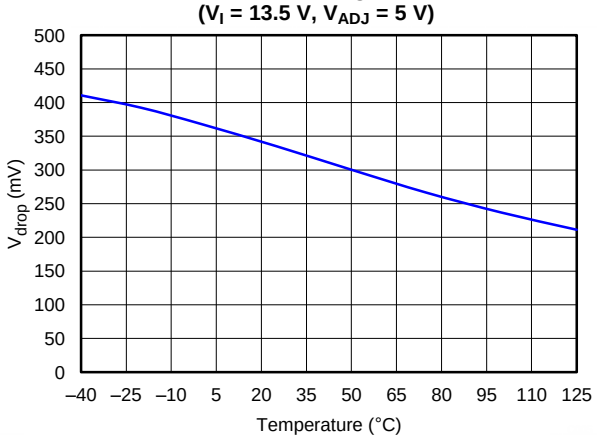



**Figure 8.**

**TRACKING ERROR vs TEMPERATURE ($V_I$ = 13.5 V, $V_{ADJ}$ = 5 V, $I_O$ = 1 mA, 50 mA)**

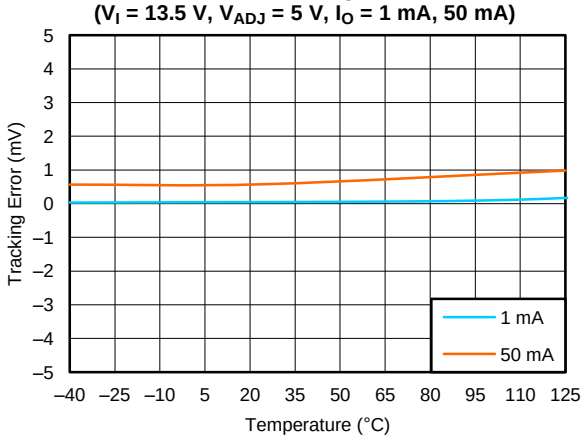



**Figure 9.**

## TYPICAL CHARACTERISTICS (continued)

**INPUT VOLTAGE vs OUTPUT VOLTAGE**

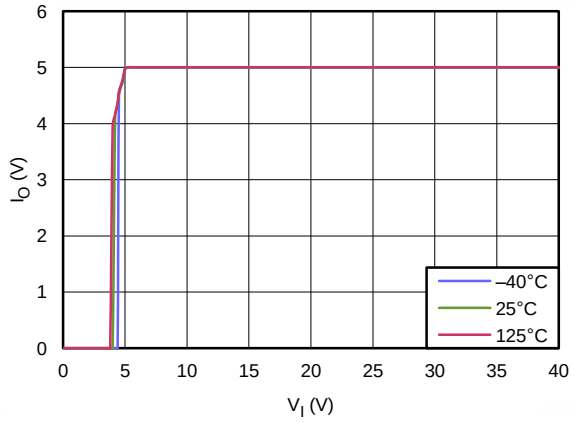



**Figure 10.**

**INPUT VOLTAGE vs OUTPUT VOLTAGE**

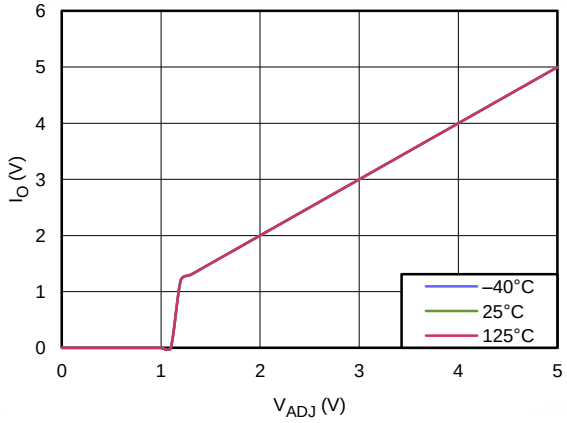



**Figure 11.**

**LINE TRANSIENT ($V_I$ = 9 to 16 V, 2.2 µF Ceramic Output Capacitor)**

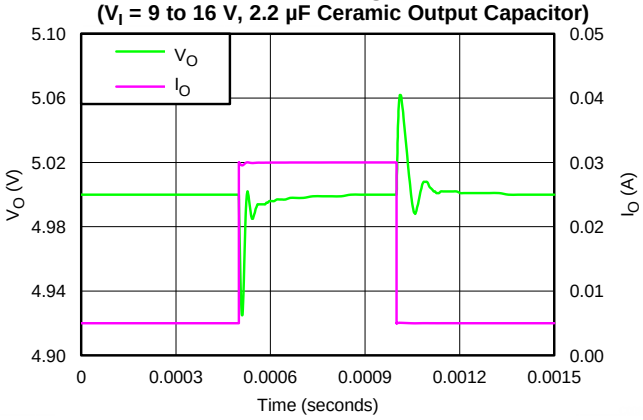



**Figure 12.**

**LOAD TRANSIENT ($I_O$ = 5 to 30 mA, 2.2 µF Ceramic Output Capacitor)**

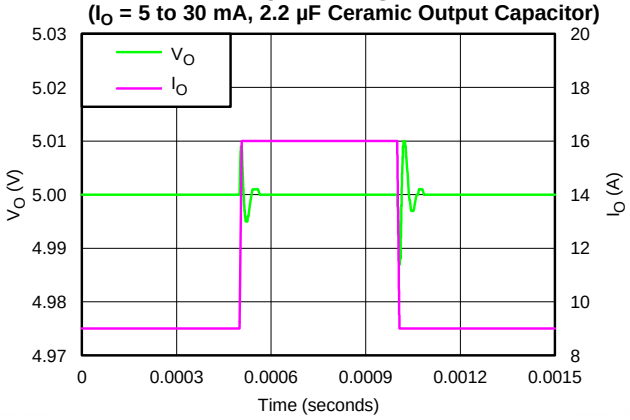



**Figure 13.**

**POWER-SUPPLY REJECTION RATIO vs FREQUENCY ($V_I$ = 13.5 V, $C_O$ = 2.2 µF, $I_{LOAD}$ = 25 mA)**

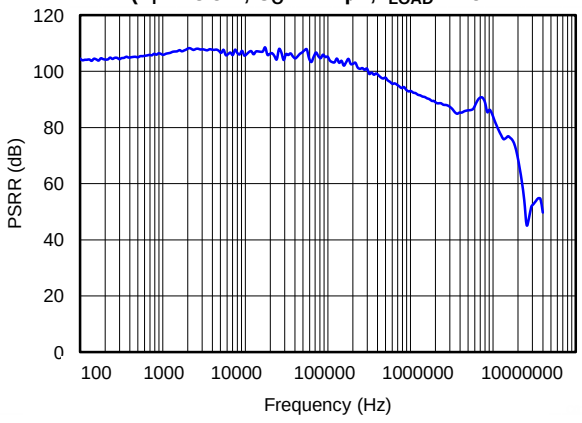



**Figure 14.**

**ESR STABILITY vs LOAD CAPACITANCE**

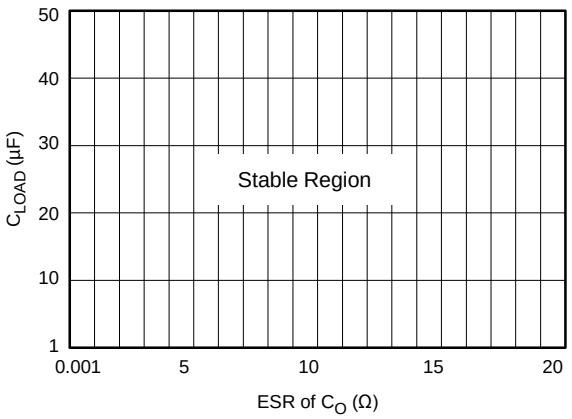



**Figure 15.**

## DETAILED DESCRIPTION

The TPS7B4250-Q1 device is a monolithic integrated low-dropout voltage tracker with ultra-low tracking tolerance. Several types of protection circuits are also integrated in the device such as output current limitation, reverse polarity protection, and thermal shutdown in case of over temperature.

### Regulated Output ($V_{OUT}$)

$V_{OUT}$ is the regulated output based on the reference voltage. The output has current limitation. During initial power up, the regulator has an incorporated soft start to control the initial current through the pass element.

### Undervoltage Shutdown

The device has an internally-fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on $V_{IN}$ drops below UVLO. This activation ensures the regulator is not latched into an unknown state during low input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up similar to a standard power-up sequence when the input voltage is above the required levels.

### Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous standard operation, the junction temperature must not exceed the TSD trip-point. If the junction temperature exceeds the TSD trip-point, the output turns off. When the junction temperature falls below the TSD trip-point minus TSD hysteresis, the output turns on again.

### $V_{OUT}$ short to Battery

The TPS7B4250-Q1 device survives a short to battery when the output is shorted to the battery as shown in Figure 16. No damage occurs to the device. A short to the battery can also occur when the device is powered by an isolated supply at a lower voltage as shown in Figure 17. In this case the TPS7B4250-Q1 supply input voltage is set at 7 V when a short to battery (14 V typical) occurs on $V_{OUT}$ which typically runs at 5 V. The reverse current flows out through $V_{IN}$ is less than 5 µA.

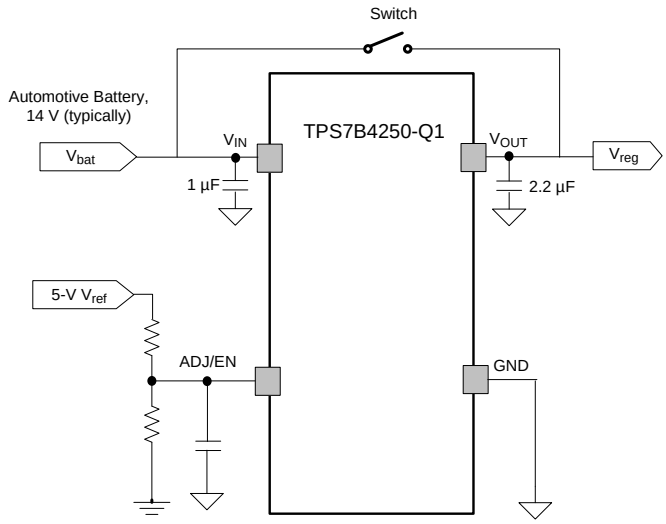



**Figure 16. Output-Voltage Short to Battery**

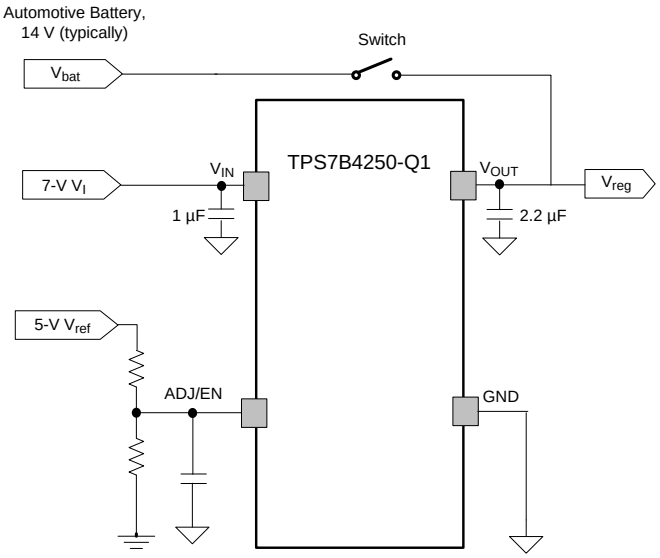



**Figure 17. Output Voltage Higher than Input**

## Tracking Regulator with ENABLE Circuit

By pulling the reference voltage of the device below 0.8 V, the IC disables and enters a sleep state where the device draws 7.5 µA (typical) from the power supply. In a real application, the reference voltage is generally sourced from another LDO voltage rail. A case where the device must be disabled without a shutdown of the reference voltage can occur. In such case, the device can be configured as shown in Figure 18. The TPS7A6650-Q1 device is a 150-mA LDO with ultra-low quiescent current that is used as a reference voltage to the TPS7B4250-Q1 device and also as a power supply to the ADC. In a configuration as shown in Figure 18, the status of the device is controlled by an MCU I/O.

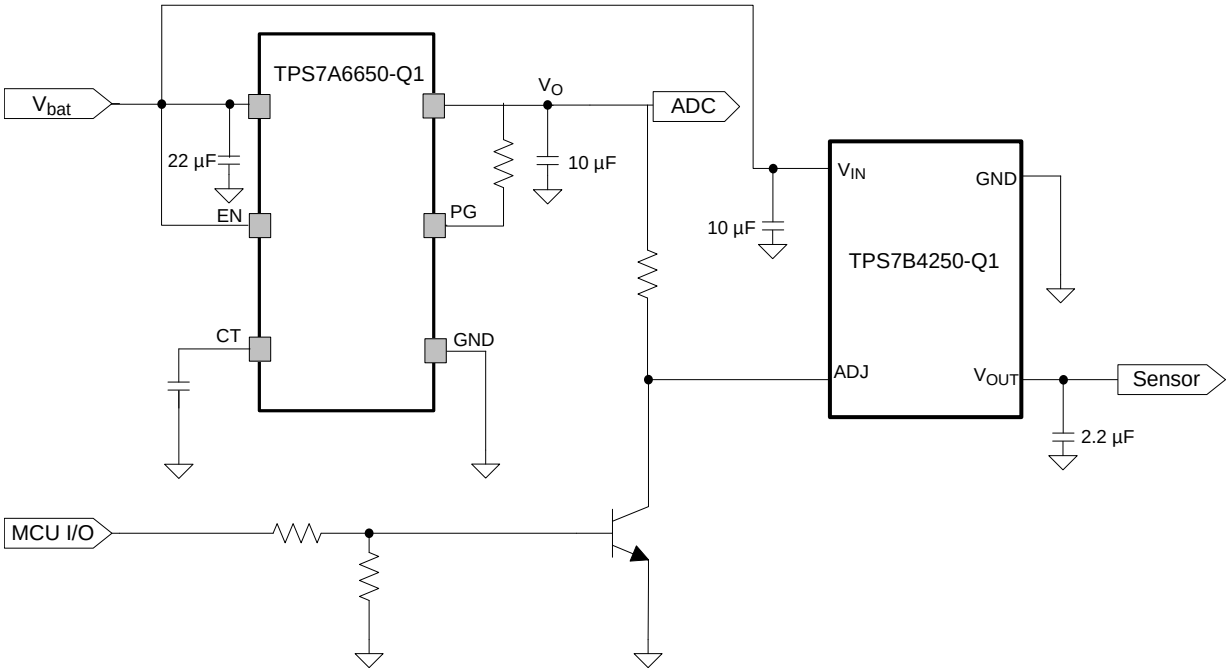



**Figure 18. Tracking LDO With Enable Circuit**

## External Capacitors

An input capacitor, $C_I$, is recommended to buffer line influences. Connect the capacitors close to the IC terminals.

The output capacitor for the TPS7B4250-Q1 device is required for stability. Without the output capacitor, the regulator oscillates. The actual size and type of the output capacitor can vary based on the application load and temperature range. The effective series resistance (ESR) of the capacitor is also a factor in the IC stability. The worst case is determined at the minimum ambient temperature and maximum load expected. To ensure stability of TPS7B4250-Q1 device, the device requires an output capacitor between 1 µF and 50 µF with an ESR range between 0.001 Ω and 20 Ω that can cover most types of capacitor ESR variation under the recommend operating conditions. As a result, the output capacitor selection is flexible.

The capacitor must also be rated at all ambient temperature expected in the system. To maintain regulator stability down to –40°C, use a capacitor rated at that temperature.

## Power Dissipation and Thermal Considerations

Device power dissipation is calculated with Equation 1.

$$P_D = I_O \times (V_I - V_O) + I_Q \times V_I \quad (1)$$

where

- $P_D$ = continuous power dissipation
- $I_O$ = output current
- $V_I$ = input voltage
- $V_O$ = output voltage
- $I_Q$ = quiescent current

As $I_Q \ll I_O$, the term $I_Q \times V_I$ in Equation 1 can be ignored.

For a device under operation at a given ambient air temperature ($T_A$), calculate the junction temperature ($T_J$) with Equation 2.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (2)$$

where

- $\theta_{JA}$ = junction-to-junction-ambient air thermal impedance

A rise in junction temperature because of power dissipation can be calculated with Equation 3.

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D) \quad (3)$$

For a given maximum junction temperature ($T_{JM}$), the maximum ambient air temperature ($T_{AM}$) at which the device can operate can be calculated with Equation 4.

$$T_{AM} = T_{JM} - (\theta_{JA} \times P_D) \quad (4)$$

# LAYOUT INFORMATION

## Package Mounting

Solder-pad footprint recommendations for the TPS7B4250-Q1 device are available at the end of this data sheet and at www.ti.com.

## Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, TI recommends to design the board with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7B4250 evaluation board, available at www.ti.com.

## Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C which allows the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The internal protection circuitry of the TPS7B4250-Q1 device has been designed to protect against overload conditions. The circuitry was not intended to replace proper heat-sinking. Continuously running the TPS7B4250-Q1 device into thermal shutdown degrades device reliability.

## REVISION HISTORY

**Changes from Original (October 2013) to Revision A** **Page**

- Changed CDM ESD Classification level from C3B to C4 throughout document ..... 1
- Changed $V_{OUT}$ min value from –0.3 to –1 in the *ABSOLUTE MAXIMUM RATINGS* table ..... 2
- Changed HBM absolute maximum rating from 2 kV to 4 kV ..... 2
- Added transient current flow to ESD rating in the *ABSOLUTE MAXIMUM RATINGS* table ..... 2
- Deleted relevant ESR value from *RECOMMENDED OPERATING CONDITIONS* table ..... 2
- Added grater-than-or-equal-to (≥) value to $V_{ADJ/EN}$ in condition statement of the *ELECTRICAL CHARACTERISTICS* table ..... 3
- Added $V_{ADJ}$ = 1.5 V to both test conditions for $V_{UVLO}$ parameter in the *ELECTRICAL CHARACTERISTICS* table ..... 3
- Changed max value for load regulation parameter from 3 to 4 in the *ELECTRICAL CHARACTERISTICS* table ..... 3
- Changed max value for the current consumption test condition where $I_O$ = 0.5 mA from 80 to 90 in the *ELECTRICAL CHARACTERISTICS* table ..... 3
- Added the TPS7B4250 block diagram ..... 5
- Added the *DETAILED DESCRIPTION* section ..... 8

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7B4250QDBVQ1 | PREVIEW | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | |
| TPS7B4250QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | PA3Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

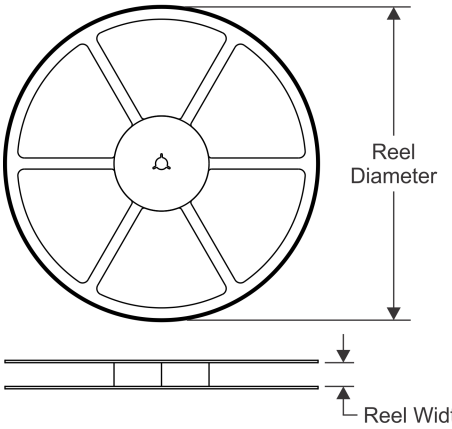
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

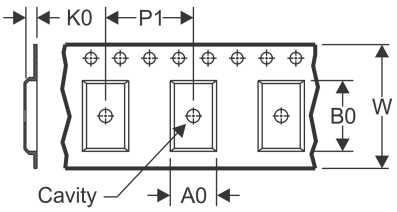
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

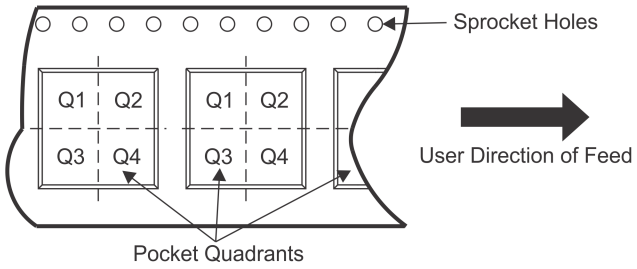



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

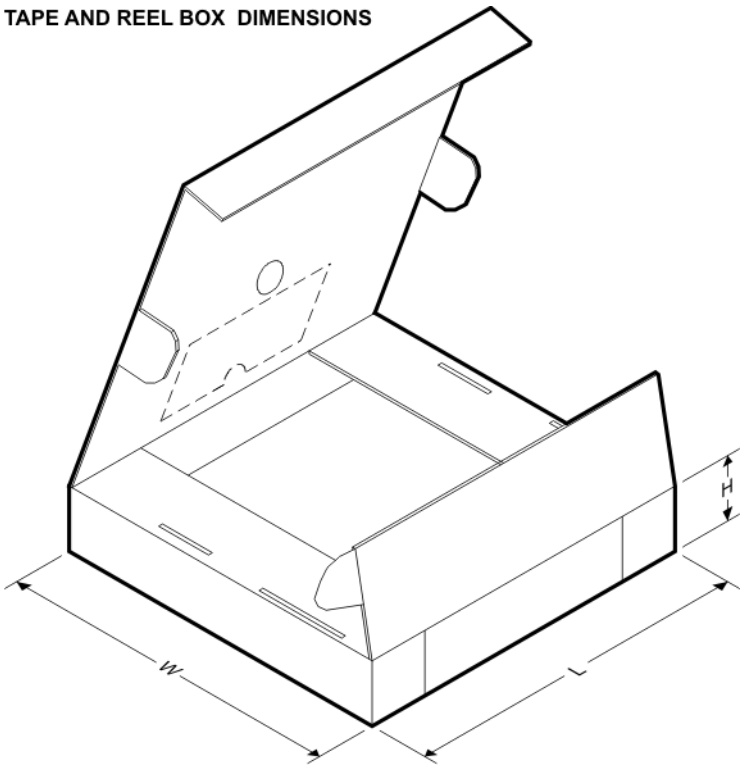
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7B4250QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

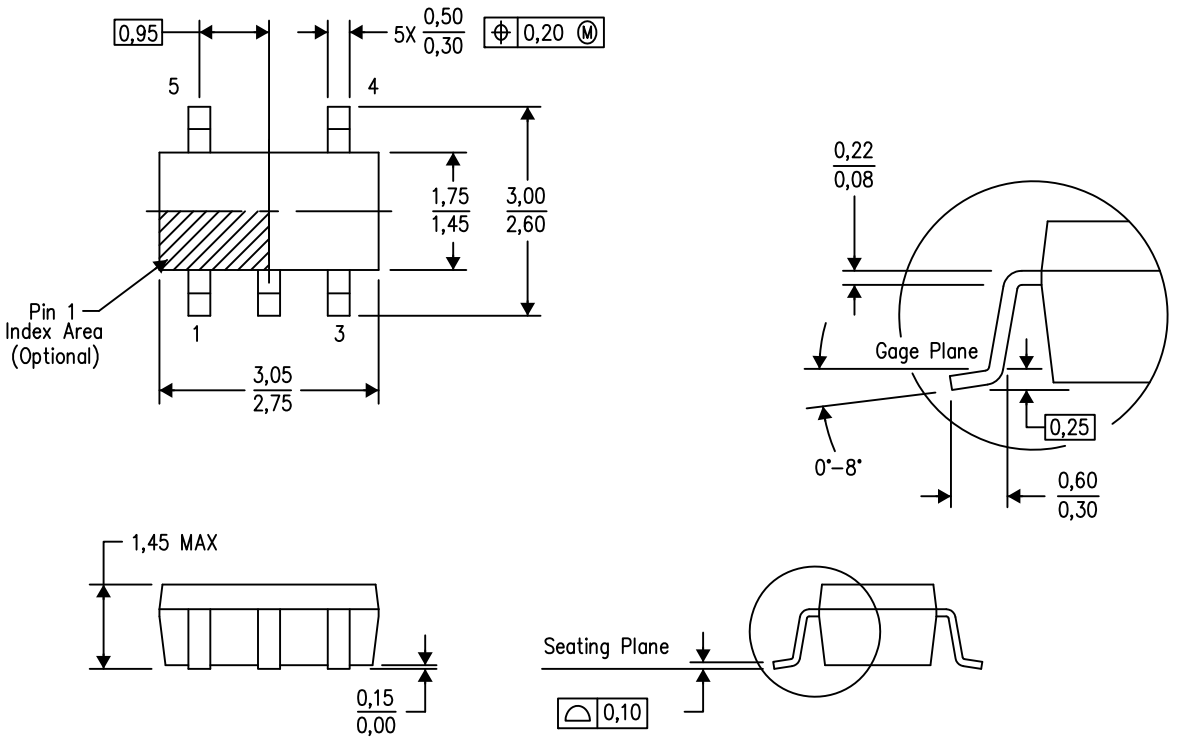
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7B4250QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 190.0 | 190.0 | 30.0 |

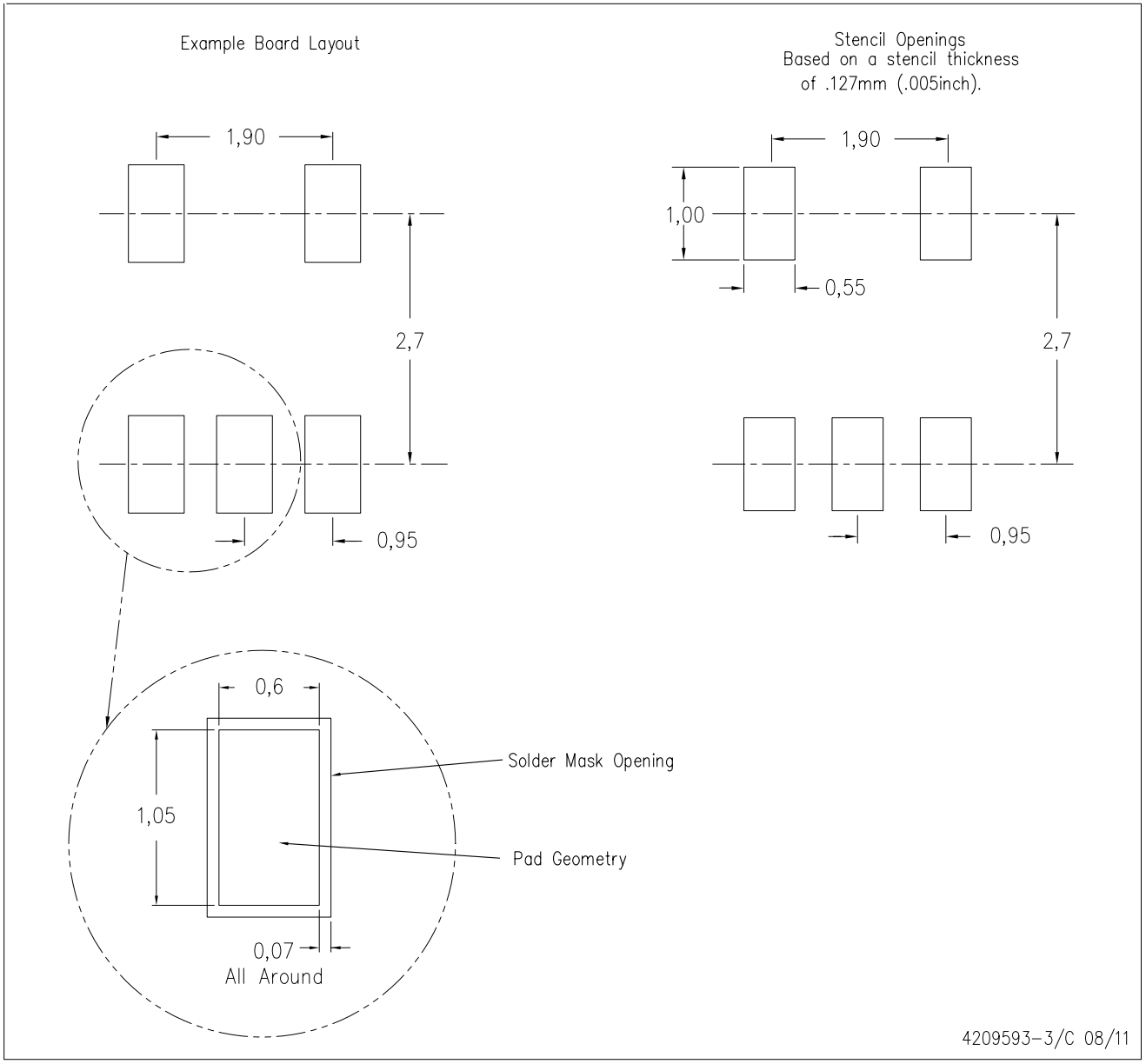
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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